ECT601– Digital CMOS ICs – 3 (3L+0P)

Process flow and masking steps for MOS and CMOS technologies, Lambda based design rules- Electrical behavior of MOS transistors; Latch up in CMOS technology.

Layer properties of various conducting layers in MOS technology (diffusion, poly-silicon and metal): Sheet resistance, relative capacitance.

Fundamental time constant (τ) for a technology.

Design and analysis of NMOS (enhancement and depletion) and CMOS inverters; rationing of transistor size, logic threshold, logic low voltage level, rise and fall of delays.

Design of basic gates in NMOS technology; CMOS logic design styles: static CMOS logic (AND, NOR gates), complex gates, domino logic, pseudo NMOS logic, clocked CMOS (C^2MOS) logic.

Structured logic design: programmable arrays.

Design of latches and flip-flops, static memory cell and dynamic memory cell.

Sense amplifier- necessity, design, and influence of Sense Amplifier on cell Architecture.

MOS scaling theory and scaling of interconnection.

References:

1. Sung-Mo Kang & Yusuf Leblebici, **CMOS Digital Integrated Circuits Analysis and Design**, McGraw-Hill, 1998.

2. Neil H.E.Weste and Kamran Eshraghian, **Principles of CMOS VLSI Design**, Addison Wesley, 1998.

3. Rabaey et al., **Digital Integrated Circuits**, Pearson India, 2002.

4. K. Martin, **Digital Integrated circuit design**, Oxford University press, 2001.

5. A. Mukherji, **Introduction to nMOS and CMOS VLSI system design**, Prentice Hall Inc., 1986.

6. C. Mead and L. Conway, **Introduction to VLSI systems**, Addison Wesley, 1986.

7. Glasser and Dobberpuhl, **Design and analysis of VLSI circuits**, Addison Wesley, 1985.